FORM 6-K

SECURITIES AND EXCHANGE COMMISSION

Washington, D.C. 20549

For the month of December 2006

TOWER SEMICONDUCTOR LTD.
(Translation of registrant's name into English)

RAMAT GAVRIEL INDUSTRIAL PARK
P.O. BOX 619, MIGDAL HAEMEK, ISRAEL 23105
(Address of principal executive offices)

Indicate by check mark whether the registrant files or will file annual reports under cover Form 20-F or Form 40-F.

Form 20-F [X] Form 40-F [_]

Indicate by check mark whether the registrant by furnishing the information contained in this Form is also thereby furnishing the information to the Commission pursuant to Rule 12g3-2(b) under the Securities Exchange Act of 1934.

Yes [_] No [X]

On December 12, 2006, Tower Semiconductor announced it expands High-Voltage Technology offering with Synopsys' Hercules PVS, attached hereto is a copy of the press release.

This Form 6-K is being incorporated by reference into all effective registration statements filed by us under the Securities Act of 1933.

SIGNATURES

Pursuant to the requirements of the Securities Exchange Act of 1934, the registrant has duly caused this report to be signed on its behalf by the undersigned, thereunto duly authorized.

TOWER SEMICONDUCTOR LTD.

Date: December 12, 2006

By: /s/ Nati Somekh Gilboa

Nati Somekh Gilboa
Corporate Secretary

TOWER SEMICONDUCTOR EXPANDS HIGH-VOLTAGE TECHNOLOGY OFFERING WITH SYNOPSYS' HERCULES PVS

NEW RULE FILES COMPLEMENT TOWER'S RELEASE OF HIGH-VOLTAGE TECHNOLOGY

MOUNTAIN VIEW, CALIF., AND MIGDAL HAEMEK, ISRAEL, DECEMBER 12, 2006 - Synopsys, Inc., a world leader in semiconductor design software, and Tower Semiconductor Ltd. (Nasdaq:TSEM, TASE:TSEM), a pure-play independent specialty foundry, today announced that Synopsys' Hercules(TM) Physical Verification Suite (PVS) rule files are now available for Tower Semiconductor's release of 180-nanometer (nm) high-voltage technology. The availability of Hercules rule files for both design rule checking (DRC) and layout versus schematic (LVS) on this specialized process is the result of close cooperation between the two companies. Hercules rule files are also supported in Tower's standard logic technology processes.

"Tower's continued support of Hercules PVS for sign-off verification enables our customers to continue working in the Synopsys design environment for our specialized technology offering," said Yaakov Milstain, vice president and general manager for design services at Tower. "This joint endeavor is evidence of our strong relationship with Synopsys, one of the leading EDA providers."

The Hercules DRC rule file development, including support for specialized 180nm high-voltage devices, has been qualified for sign-off using a rigorous set of specialized test cases. Hercules LVS can also be used with Synopsys' Star-RCXT(TM) extraction solution to merge highly accurate parasitic data with the schematic-level devices. This unique capability delivers greater simulation accuracy while allowing circuit designers to design and analyze circuits at a familiar level of detail.

"The availability of Hercules PVS rule files for Tower's high-voltage technology demonstrates the broadening foundry support for Hercules PVS on specialized processes," said Anantha Sethuraman, vice president of marketing, Design for Manufacturing, at Synopsys. "Qualification by foundries such as Tower Semiconductor enables our mutual customers to benefit from higher DRC performance and a proven transistor flow."

ABOUT SYNOPSYS DFM

With its design for manufacturing (DFM) tools, Synopsys is expanding on what is already the industry's most comprehensive DFM solution that spans from RTL to silicon. Synopsys' DFM product family addresses critical manufacturability and yield issues with the following products: IC Compiler physical design solution, PrimeYield LCC, PrimeYield CMP and PrimeYield CAA, Hercules(TM) PVS, Proteus OPC, CATS(R) mask data preparation product, SiVL(R) lithography verification tool, patented PSM technology, and physics-based TCAD suite of simulation products. Synopsys' Manufacturing Yield Management (MYM) solutions extend directly into the fab, providing customers real time access to yield data and the analysis capability needed to reduce random, systematic and parametric defects.

ABOUT SYNOPSYS

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chip (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys has its headquarters in Mountain View, Calif., and has offices in more than 60 locations throughout North America, Europe, and Asia. Visit Synopsys online at http://www.synopsys.com.

ABOUT TOWER SEMICONDUCTOR

Tower Semiconductor Ltd. is a pure-play independent specialty wafer foundry established in 1993. The company manufactures integrated circuits with geometries ranging from 1.0 to 0.13-micron; it also provides complementary technical services and design support. In addition to digital CMOS process technology, Tower offers advanced non-volatile memory solutions, mixed-signal & RF-CMOS, and CMOS image-sensor technologies. To provide world-class customer service, the company maintains two manufacturing facilities: Fab 1 has process technologies from 1.0 to 0.35 micron and can produce up to 16,000 150mm wafers per month. Fab 2 features 0.18 and 0.13-micron, standard and specialized process technologies, and has the current capacity of up to 15,000 200mm wafers per month. Tower's Web site is located at http://www.towersemi.com.

SAFE HARBOR

This press release includes forward-looking statements, which are subject to risks and uncertainties. Actual results may vary from those projected or implied by such forward-looking statements. A complete discussion of risks and uncertainties that may affect the accuracy of forward-looking statements included in this press release or which may otherwise affect our business is included under the heading "Risk Factors" in our most recent Annual Report on Form 20-F, Forms F-1, F-3 and 6-K, as were filed with the Securities and Exchange Commission and the Israel Securities Authority. We do not intend to update, and expressly disclaim any obligation to update, the information contained in this release.

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