FORM 6-K

SECURITIES AND EXCHANGE COMMISSION

Washington, D.C. 20549

For the month of November 2005 No.3

TOWER SEMICONDUCTOR LTD.
(Translation of registrant's name into English)

P.O. BOX 619, MIGDAL HAEMEK, ISRAEL 23105
(Address of principal executive offices)

Indicate by check mark whether the registrant files or will file annual reports under cover Form 20-F or Form 40-F.

Form 20-F [X] Form 40-F [_]

Indicate by check mark whether the registrant by furnishing the information contained in this Form is also thereby furnishing the information to the Commission pursuant to Rule 12g3-2(b) under the Securities Exchange Act of 1934.

Yes [_] No [X]

On November 14, 2005, the Registrant announced that it collaborates with Cadence to deliver optimized reference flow for specialty technology processes. Attached hereto is a copy of the press release.

This Form 6-K is being incorporated by reference into all effective registration statements filed by us under the Securities Act of 1933.

SIGNATURES

Pursuant to the requirements of the Securities Exchange Act of 1934, the registrant has duly caused this report to be signed on its behalf by the undersigned, thereunto duly authorized.

TOWER SEMICONDUCTOR LTD.

Date: November 14, 2005

By: /S/ Nati Somekh Gilboa

Nati Somekh Gilboa
Corporate Secretary

TOWER SEMICONDUCTOR COLLABORATES WITH CADENCE TO DELIVER OPTIMIZED REFERENCE FLOW FOR SPECIALTY TECHNOLOGY PROCESSES

DESIGN CHAIN COLLABORATION ACCELERATES SANDISK'S TIME-TO-MARKET

MIGDAL HAEMEK, ISRAEL, NOVEMBER 14, 2005 - Tower Semiconductor Ltd. (Nasdaq: TSEM; TASE: TSEM) today announced a collaboration with Cadence Design Systems, Inc. (NASDAQ: CDNS) to deliver a reference flow targeting system-on-chip (SoC) designs at 0.18-micron using Tower's CMOS mixed-signal process. In addition, Tower has joined the Cadence foundry partner program to enhance the combined offering of solutions to the customer.

The reference flow utilizes the Cadence(R) Encounter(R) digital IC design platform, the Virtuoso(R) custom IC design platform and the Incisive(R) functional verification platform, and libraries from Tower and third-party providers. This RTL-to-GDSII reference flow optimizes the design chain by enabling a low-risk, predictable path from design to volume production. The flow reduces iterations in the design phase and improves accuracy through model optimization.

"We were impressed by the way that Cadence's Virtual Computer Aided Design (VCAD) Services built a reference flow and implemented it within Tower's technology, ensuring consistency throughout all design steps and enabling the full potential of Tower's 0.18-micron process and Cadence's software," said Geoff Gongwer, senior director, ASIC and CAD at SanDisk Corporation (Nasdaq: SNDK). "Using the reference flow on a critical design enabled us to avoid unforeseen physical design issues and to achieve silicon success at Tower."

"The increased mixed-signal content in today's SoCs requires access to detailed and accurate process information during the design phase," said Jan Willis, senior vice president, Industry Alliances, at Cadence. "Collaboration through the design chain produces the process design kits and libraries that provide designers with this information for implementing their design. This jointly-developed reference flow with Tower provides a fully validated methodology that will improve the productivity of customers designing with Cadence software targeting the Tower 0.18-micron process."

"The development of this reference flow is another step in the ongoing collaboration between Tower and Cadence," said Yaakov Milstain, vice president and general manager of design services at Tower Semiconductor Ltd. "The reference flow, based on Cadence design platforms, enables our customers to realize a much faster path to production silicon using Tower's leading-edge specialty process technologies."

Tower has qualified Cadence as part of the Tower Authorized Design Center (TADC) program to expand customer access to Cadence's leading design services capabilities.

AVAILABILITY

The Reference Flow is available through Tower. Contact either your Tower or Cadence account manager for more information.

Additional details about the foundry partner program can be found at www.cadence.com

ABOUT TOWER SEMICONDUCTOR LTD.

Tower Semiconductor Ltd. is a pure-play independent specialty foundry established in 1993. The company manufactures integrated circuits with geometries ranging from 1.0 to 0.13 micron; it also provides complementary technical services and design support. In addition to digital CMOS process technology, Tower offers advanced non-volatile memory solutions, mixed-signal, RF-CMOS and CMOS image-sensor technologies. To provide world-class customer service, the company maintains two manufacturing facilities: Fab 1 has process technologies from 1.0 to 0.35-micron and can produce up to 16,000 150mm wafers per month. Fab 2 features 0.18-micron and below standard and specialized process technologies, and has the current capacity of up to 15,000 200mm wafers per month. Tower's Web site is located at www.towersemi.com.

Safe Harbor

THIS PRESS RELEASE INCLUDES FORWARD-LOOKING STATEMENTS, WHICH ARE SUBJECT TO RISKS AND UNCERTAINTIES. ACTUAL RESULTS MAY VARY FROM THOSE PROJECTED OR IMPLIED BY SUCH FORWARD-LOOKING STATEMENTS. POTENTIAL RISKS AND UNCERTAINTIES INCLUDE, WITHOUT LIMITATION, RISKS AND UNCERTAINTIES ASSOCIATED WITH MARKET DEMAND FOR 0.18-MICRON TECHNOLOGY MANUFACTURING SERVICES. A MORE COMPLETE DISCUSSION OF RISKS AND UNCERTAINTIES THAT MAY AFFECT THE ACCURACY OF FORWARD-LOOKING STATEMENTS INCLUDED IN THIS PRESS RELEASE OR WHICH MAY OTHERWISE AFFECT OUR BUSINESS IS INCLUDED UNDER THE HEADING "RISK FACTORS" IN OUR MOST RECENT ANNUAL REPORT ON FORM 20-F AND IN OUR FORMS 6-K AND F-2, AS AMENDED, AS WERE FILED WITH THE SECURITIES AND EXCHANGE COMMISSION AND THE ISRAEL SECURITIES AUTHORITY.

TOWER CORPORATE CONTACT	TOWER AGENCY CONTACT
Michael Axelrod	Mary Curtis
Tower Semiconductor USA	Pacifico Inc.
(408) 330-6871	(408) 293-8600
pr@towersemi.com	mcurtis@pacifico.com