

FORM 6-K

SECURITIES AND EXCHANGE COMMISSION

Washington, D.C. 20549

For the month of July 2003

TOWER SEMICONDUCTOR LTD.
(Translation of registrant's name into English)

P.O. BOX 619, MIGDAL HAEMEK, ISRAEL 10556
(Address of principal executive offices)

Indicate by check mark whether the registrant files or will file annual reports under cover Form 20-F or Form 40-F.

Form 20-F Form 40-F
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Indicate by check mark whether the registrant by furnishing the information contained in this Form is also thereby furnishing the information to the Commission pursuant to Rule 12g3-2(b) under the Securities Exchange Act of 1934.

Yes No x

On June 24, 2003, the Registrant announced the release of its 0.18 and 0.35 micron process design kits. A copy of the press release is attached hereto as Exhibit 1.

On July 2, 2003, the Registrant announced the hiring of Rafi Nave as vice president of customer services. A copy of the press release is attached hereto as Exhibit 2.

On July 9, 2003, the Registrant announced that legal action had been filed against it and certain of its directors and shareholders. A copy of the press release is attached hereto as Exhibit 3.

This Form 6-K is being incorporated by reference in all effective registration statements filed by us under the Securities Act of 1933.

SIGNATURES

Pursuant to the requirements of the Securities Exchange Act of 1934, the registrant has duly caused this report to be signed on its behalf by the undersigned, thereunto duly authorized.

TOWER SEMICONDUCTOR LTD.

Date: July 22, 2003

By: /s/ Sheldon Krause

Sheldon Krause
Assistant Secretary

MIGDAL HAEMEK, Israel & SAN JOSE, Calif--June 24, 2003--

Cadence-Developed PDKs Reduce Risk and Simplify the Silicon Design Process for Tower's Customers

Tower Semiconductor Ltd. (Nasdaq:TSEM), an independent pure-play wafer manufacturer, and Cadence Design Systems Inc. (NYSE:CDN), today announced the immediate availability of the new Tower TSL018 and TSL035 foundry-level Process Design Kits (PDKs) developed by Cadence Design Systems. The new PDKs eliminate the need for Tower customers to create their own "views" of the Tower technologies in their design environments, thereby reducing design time and risk. Through this development, Tower and Cadence are enabling a key component of the silicon design chain for their mutual customers.

"The ability to support custom design methodologies with silicon-validated process design kits is a strong benefit to companies working with these complex designs," said Sergio Kusevitzky, vice president of IP and design services, Tower Semiconductor. "Cadence's track record of expertise and commitment to customer support has proved to be the most effective choice for our customers."

The PDKs include a device and symbol library, technology file, physical verification decks, and design-rule-correct parameterized cells (P-cells) to automate device layout. The PDKs are compatible with the Cadence Spectre(R) models provided by Tower Semiconductor and are tailored for use in the Cadence RF/analog mixed-signal design solution consisting of AMS Designer, Composer, Analog Design Environment, Spectre/Spectre-RF, Virtuoso(R) Layout Editor and XL, Custom Router and the Assura(TM)/Diva(R) physical verification suites.

"The development work with Tower Semiconductor demonstrates our on-going commitment to the foundry market and the silicon design chain. The PDKs we have supplied provide a silicon foundation for Tower customers to design in the Tower process," said Guillaume d'Eyssautier, senior vice president and general manager, Europe, Cadence Design Systems.

About Tower Semiconductor Ltd.

Tower Semiconductor Ltd. is a pure-play independent wafer foundry established in 1993. The company manufactures integrated circuits with geometries ranging from 1.0 to 0.18 microns; it also provides complementary manufacturing services and design support. In addition to digital CMOS process technology, Tower offers advanced non-volatile memory solutions, mixed-signal and CMOS image-sensor technologies. To provide world-class customer service, the company maintains two manufacturing facilities: Fab 1 has process technologies from 1.0 to 0.35 microns and can produce up to 20,000 150mm wafers per month. Fab 2 features 0.18-micron and below process technologies, including foundry-standard technology, and will offer full production capacity of 33,000 200mm wafers per month. The Tower Web site is located at www.towersemi.com.

About Cadence

Cadence is the world's leader in electronic design technologies, methodology services, and design services. Cadence solutions are used to accelerate and manage the design of semiconductors, computer systems, networking and telecommunications equipment, consumer electronics, and a variety of other electronics-based products. With approximately 5,200 employees and 2002 revenues of approximately \$1.3 billion, Cadence has sales offices, design centers, and research facilities around the world. The company is headquartered in San Jose, Calif, and traded on the New York Stock Exchange under the symbol CDN. More information about the company, its products and services is available at www.cadence.com.

Cadence and the Cadence logo are registered trademarks and Virtuoso Custom Design, Virtuoso-XL and Cadence Chip Assembly Router are trademarks of Cadence Design Systems, Inc. All other trademarks are the property of their respective owners.

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TOWER REINFORCES COMMITMENT TO CUSTOMER SERVICE WITH NEW APPOINTMENT
INTEL VETERAN RAFI NAVE TO SERVE AS VP OF CUSTOMER SERVICES

MIGDAL HAEMEK, ISRAEL - July 2, 2003 - Tower Semiconductor Ltd. (NASDAQ: TSEM; TASE: TSEM) announced today that Rafi Nave will join the company as vice president of customer services. This appointment will take effect in mid-August 2003.

In this position, Nave will oversee all areas of customer service, including account management, project management, IP and design services, the VLSI design center and customer support. He will report directly to Carmel Vernia, chairman of the board and CEO of Tower. Nave is the first senior appointment since Vernia joined the company a month ago.

"Tower has long been recognized and rewarded by customers for providing exceptional service and support," said Vernia. "Taking our customer-service organization to new heights of achievement is essential to enhancing our global market position, and I am confident that Rafi is the person to lead that effort. With over 20 years of experience gained from working at Intel, he is familiar with customer needs and knows how to provide customers with the best possible service solutions. Rafi is a welcome addition to the Tower team."

Creating the position of vice president of customer services is the most recent action that Tower has taken as part of its broader customer relationship management initiative. Earlier this year, Tower opened a new office near Boston to support customers in the eastern United States and hired Harold Blomquist to direct the company's global business development activities from Israel and the United States. As well, the company has built an extensive IP portfolio and has developed various design support services to make it easier for customers to achieve first-time silicon success.

"Having worked in the semiconductor industry for most of my career, I have watched with great interest Tower's inception and evolution. The company has overcome myriad obstacles, including the most recent downturn, through the intelligence, hard work and perseverance of its people. Tower has reached a very exciting juncture in its history, and I am honored that I will have the opportunity to play a key role in its next phase of development and growth," said Nave.

Nave joins Tower after six years of serving as vice president of R&D for NDS Group (NASDAQ: NNDS), where he managed a group of 300 engineers and scientists. Prior to that, he spent most of his career at Intel Corporation in a variety of positions of increasing responsibility. He started as a chip design engineer, and then went on to manage the

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TOWER REINFORCES COMMITMENT TO CUSTOMER SERVICE WITH NEW APPOINTMENT
PAGE 2 OF 2

development of Intel's family of 8XX87 math co-processors. Next, he served for five years as the general manager of Intel's design center in Israel, employing 200 engineers and designing Intel's leading products. Nave earned master's and bachelor's degrees in electrical engineering (with honors) from the Technion in Haifa, Israel.

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TOWER SEMICONDUCTOR LTD. ANNOUNCES
IT HAS LEARNED THAT ACTION HAS BEEN FILED AGAINST IT

MIGDAL HAEMEK, ISRAEL -- JULY 09, 2003 -- Tower Semiconductor Ltd. (NASDAQ: TSEM; TASE: TSEM) today announced that it has learned, based on a press release issued to the news services, that an action has been filed in the United States District Court for the Southern District of New York on behalf of the holders of Tower Semiconductor Ltd., against Tower and certain of its directors and shareholders, asserting claims arising under Sections 14(a) and 20(a) of the Securities Exchange Act of 1934 and Rule 14a-9 promulgated thereunder.

While the company has not received a copy of the lawsuit, based on the information appearing in the press release issued today, it believes that this lawsuit is without merit.

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SAFE HARBOR

This press release includes forward-looking statements, which are subject to risks and uncertainties. Our actual results may vary from those projected or implied by such forward-looking statements. Potential risks and uncertainties include, without limitation, risks and uncertainties associated with (i) Our need to complete our 2003 financing package with our banks, which is a condition to receipt of the remainder of the first installment of our fifth milestone payment from our wafer and equity investors in the amount of \$11.2 million, (ii) raising at least \$26 million of additional funding for Fab 2 before the end of 2003, which is a condition to completion of the fifth milestone investment by our major wafer and equity partners in the amount of \$16.4 million, (iii) obtaining the approval of the Israeli Investment Center to extend the five-year investment period under our Fab 2 approved enterprise program and of amendments to our modified business plan, (iv) with the lawsuit filed against us in the southern district of New York, (v) market acceptance and competitiveness of the products to be manufactured by us for customers using these technologies, as well as obtaining additional business from new and existing customers, (vi) our need to renegotiate our Fab 2 credit facility to

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TOWER SEMICONDUCTOR LTD. ANNOUNCES FIRST QUARTER OF 2003 RESULTS
PAGE 2 OF 2

extend the deadlines by which we were and are required to meet the fifth and sixth milestones, which, in the absence of a renegotiated agreement, would result in an event of default under the credit facility in which event our banks would have the right to call our loans and exercise their liens against our assets and we would most likely face claims from our wafer partners, financial investors and the Investment Center, (vii) our ability to obtain additional financing for the Fab 2 project from equity and/or wafer partners, the Israeli Investment Center, our banks, and/or other sources, as required under the Fab 2 business plan and pursuant to our agreements with our wafer and equity partners, banks and the Israeli Investment Center, (viii) ramp-up of production at Fab 2, (ix) completion of the development and/or transfer of advanced process technologies to be utilized in our existing facility and in Fab 2, (x) conditions in the market for foundry manufacturing services and for semiconductor products generally and (xi) possible loss of our exclusive foundry license with Saifun if we fail to meet certain sales levels and other conditions. A more complete discussion of risks and uncertainties that may affect the accuracy of forward-looking statements included in this press release or which may otherwise affect our business is included at "Risk Factors" in our most recent Annual Report on Form 20-F, as filed with the Securities and Exchange Commission and the Israel Securities Authority.

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